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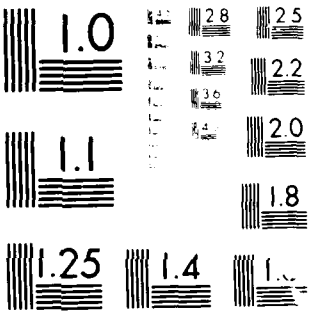
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DIELECTRIC SPECTROSCOPY OF SEMICONDUCTORS

1ST REPORT FOR

US ARMY GRANT DAJA 45-87-C-0011

starting July 15, 1987

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ABSTRACT

Dielectric studies are reported on two Schottky barriers on n-type silicon of 10 and $3\ 10^3$ Ωcm room temperature resistivity, and also on an p-n junction on 10^3 Ωcm p-type silicon. The response of all three in the frequency range 0.01 - 10^4 Hz shows the presence of a loss peak which is slightly broader than Debye, and also a dc process, with further complicating features in the case of the Schottky barrier on high-resistivity silicon. These include the appearance of a low-frequency dispersion or a negative capacitance which are strongly dependent on relatively small forward or reverse bias. Several of these features resemble the behaviour of previously investigated GaAs Schottky diodes and the important conclusion is reached that these effects are not simply the consequences of the compound nature of the semiconductor in question but are the results of electrochemical processes at the semiconductor - metal interfaces.

INTRODUCTION

The study of the Dielectric Spectroscopy of Semiconductors (DSS) has been supported by the previous US Army grant **DAJA 37-81-C-0773** in the years 1982 - 1985 and there has then been a gap of over two years before the finalising of the present second phase of the grant, starting in June 1987. The first phase has resulted in the publication of the following papers :

A K Jonscher and C Pickup, "Evidence from dielectric spectroscopy for 'electronic phase transitions' in semi-insulating Gallium Arsenide", JPhysC:Solid StatePhysics **18**, 343-349 (1985)

A K Jonscher, C Pickup and S S H Zaidi, "Dielectric spectroscopy of semi-insulating gallium arsenide, Semiconductor Sci & Techn., **1**, 71-92 (1986)

A K Jonscher and T J McCarthy, "Admittance spectroscopy of silicon Zener diodes", Semiconductor Sci & Techn, **1**, 150-160 (1986)

J R Li and A K Jonscher, "Determination of trapping dynamics of semi-insulating GaAs by frequency-dependent photoconductivity", Semiconductor Sci & Techn, *2*, 233-239 (1987),

J R Li, " Frequency-domain detection of deep levels in GaAs MESFETS", Semiconductor Sci & Techn *2*, 337-339 (1987),

S S H Zaidi and A K Jonscher, "Spectroscopy of delayed electronic transitions in GaAs Schottky diodes", Semcionductor Sci & Techn, *2*, in the press.

Between them, these papers cover the principal branches of DSS, as developed in our Laboratory under the first USArmy Grant, to wit:

a) *The frequency spectrum of the "horizontal" electronic transitions in the homogeneous* bulk material corresponding to hopping conduction near the Fermi level;

b) The corresponding spectrum of "vertical " transitions involving excitation of electrons between deep levels and the conduction and valence bands, resulting in the generation and recombination of electron-hole pairs or in trapping of either species in deep levels. These transitions normally take place in the space charge regions in p-n junctions and in Schottky barriers.

c) Vertical transitions may also occur through the interfacial states at metal-semiconductor or semiconductor-insulator interfaces and these interfacial transitions have a very different spectrum from those taking place in the volume, as under b) above. The ability to distinguish between interfacial and bulk vertical transitions is one of the more promising features of the DSS technique, especially in the context of the heterostructures and low-dimensional quantum well structures.

d) A distinctively different type of spectrum is obtained if the excitation of the semiconductor *does not occur by means of* an applied periodic electric field but arises from periodically variable optical excitation generating excess charge carriers in the presence of a steady electric field. This gives rise to a frequency-dependent photocurrent which provides a Fourier transform of the familiar time-dependent decay current after the removal of a steady illumination. The advantage lies in the fact that the frequency-domain method can easily give a range of five to six powers of ten of frequency, while the time-domain method can seldom go beyond three decades because of the inevitable difficulties arising from the dark current and noise.

The common feature of many of our experimental results is their deviation, to a lesser of greater extent, from the classical Debye spectrum in the frequency domain, which corresponds to an exponential time dependence of the response of traps and deep levels under step-function excitation. The interest in this observation lies in the fact that, to all intents and purposes, the exponential dependence is the only one seriously envisaged by most accepted theories of electronic transitions in semiconductors. The furnishing of firm experimental evidence on deviations from this time dependence is therefore important in advancing our understanding of these transitions and forcing the revision of hitherto accepted theories. The other feature is that we may be able to associate the various spectral characteristics with specific impurities and imperfections in the crystalline lattice and

this may furnish a potentially important diagnostic technique for the study of semiconductors, especially those like GaAs and silicon which have relatively wide band gaps and whose general crystalline perfection is sufficiently high to make them sensitive to even very low levels of imperfections. It is this diagnostic aspect of DSS which we intend to develop further in the coming programme of study under the US Army grant.

The main purpose of the present Report is to present some hitherto unpublished data relating to medium and high resistivity silicon , involving both interfacial processes at Schottky barriers and volume processes at interface-free p-n junctions. These results throw an new light on the understanding of the DSS data and they will form the basis of further work in the coming months.

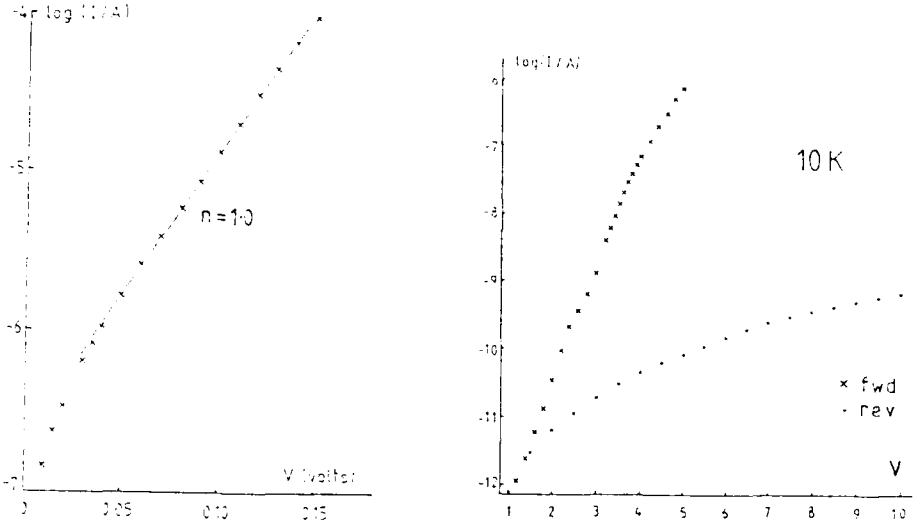

Figure 1.

The forward current-voltage characteristic of the Schottky diode at 300K, diagram a), showing the near-ideal exponential rise with voltage, with an ideality factor $n = 1.0$. Diagram b) gives the response of the same diode at 10K in forward and reverse directions , with a very strong deviation from ideality in the forward direction, with $n \cong 30$.

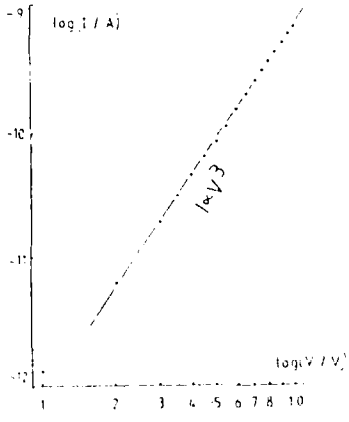

Figure 2.

The reverse current-voltage characteristic of the silicon Schottky diode at 10K, showing a power law relation with an exponent 3, at variance with normally expected behaviour , although not untypical of the response at very low temperatures.

EXPERIMENTAL DETAILS

Silicon Schottky diode

We present the DSS response data for a Schottky diode on n-type silicon of doping density of $10^{15}cm^{-3}$, with a top aluminium metallisation and an n^+ back contact, giving a barrier height of

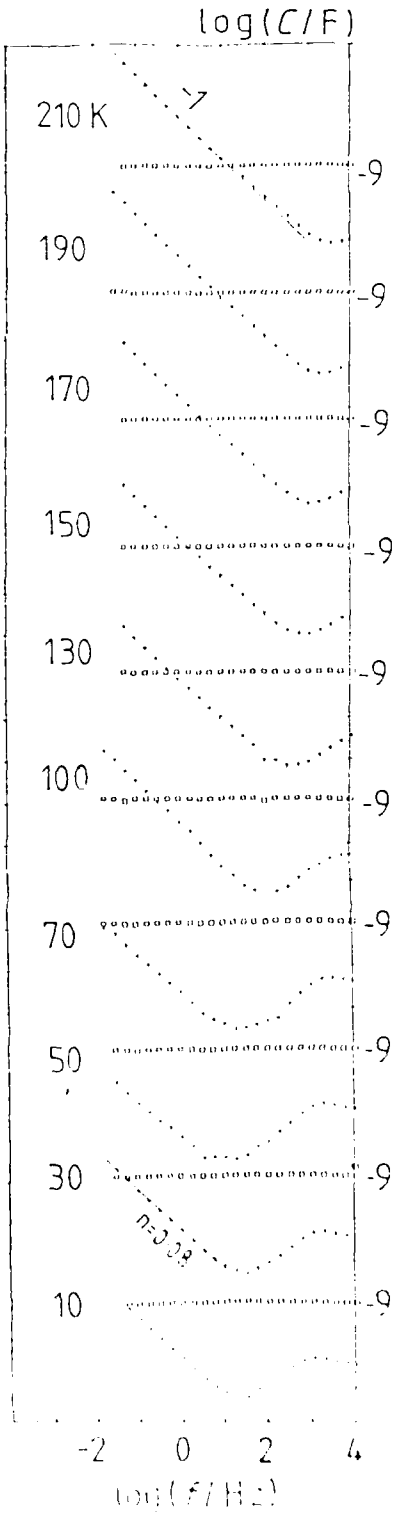

Figure 3

The dielectric response of the silicon Schottky diode plotted logarithmically against frequency in the temperature range 10-210K, showing a practically frequency-independent real part (□□□□□□) and the loss component (++++++) which has a dc - like slope of -1 at the higher temperatures and a less steep slope followed by a loss peak at the lower temperatures. The loss peak is definitely broader than the Debye shape. In this and the following spectral plots the successive sets corresponding to individual temperatures are displaced vertically by two decades for clarity and the position of 1 nF is indicated on the individual plots.

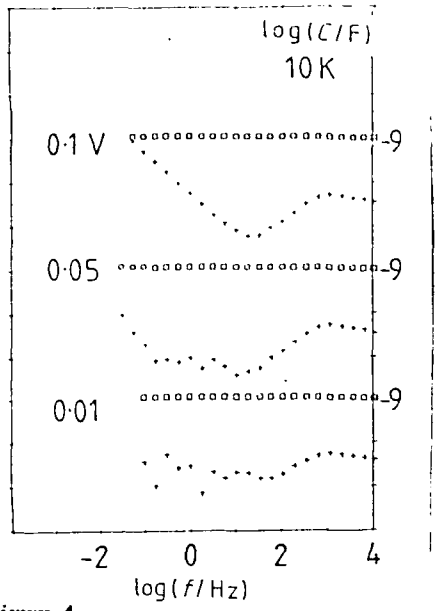

Figure 4.

The dependence of the dielectric behaviour of the silicon Schottky diode on the amplitude of the applied ac signal at 10K.

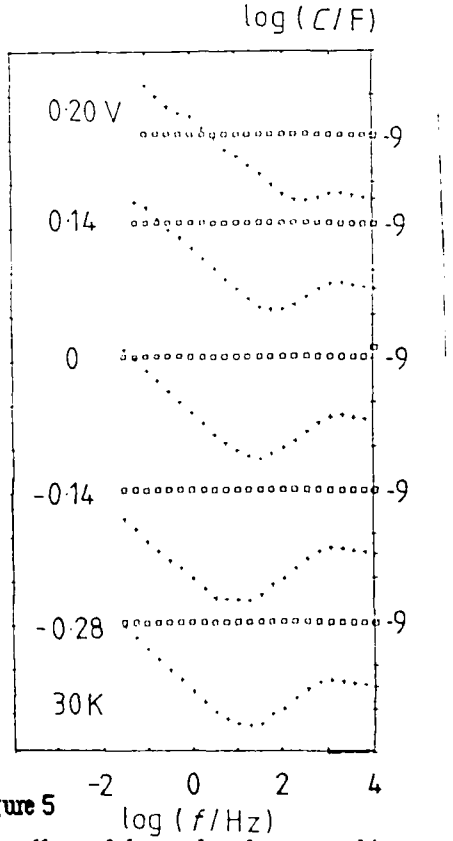

Figure 5

The effect of forward and reverse bias on the dielectric response of the Silicon Schottky diode.

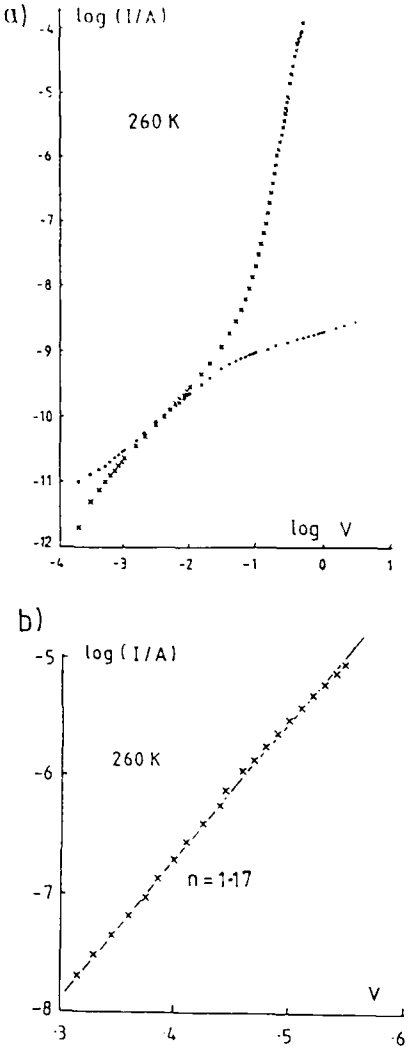

Figure 6

Diagram a) shows both branches of the I - V characteristic of the silicon surface barrier diode , diagram b) the forward branch. The ideality factor n is 1.2; suggesting an almost ideal behaviour.

0.8 eV at 77 K s determined from the C - F plot. The forward current-voltage characteristic of this diode at 300K is shown in **Figure 1a)**, where the semi-logarithmic plot gives an ideality factor in the current voltage characteristic $I \propto \exp(eV/nkT)$ of $n = 1.0$, i.e. a practically ideal response at voltages in excess of some 50 mV. The corresponding characteristics at 10K are shown in **Figure 1b)** with a strongly exponentially rising forward current but with an ideality factor of over 30 - this is not uncommonly found in semiconductor diodes at low temperatures and is evidence for the fact that the conventional theory is not applicable under these extreme conditions. The reverse characteristic gives a power law $I \propto F^3$. The $1/C^2$ vs F dependence at 77K is shown in **Figure 2** giving the carrier density of 1.3×10^{15} cm^{-3} and barrier height of 0.8 eV at that temperature.

The general conclusion from these data is that the Schottky diode in question is a reasonably well-behaved one which may be regarded as representative of its class. The dielectric response of this diode at temperatures in the range 10-210Kare shown in **Figure 3** with the capacitance being practically "flat" in the entire frequency range and the loss showing a prevailing ω^{-1} tendency at low frequencies , with a well defined loss peak appearing at the lower temperatures. A closer look at the loss data reveals that the -1 slope does not continue below the intersection with the real part, where its slope deviates markely from from that value and becomes as low as-0.6 at the lowest temperatures. This behaviour is reminiscent of similar phenomena reported for Galium Arsenide Schottky diodes by Zaidi and Jonscher in the reference cited in the Introduction. The implication is that at those temperatures the diode does not follow the dc response at low frequencies and instead that some form of Low-Frequency Dispersion (LFD) sets in. In LFD the complex capacitance follwos the "universal" law

$$\tilde{C}(\omega) = C'(\omega) - iC''(\omega) \propto (i\omega)^{n-1} \qquad (1)$$

where the exponent n takes on values close to zero. This implies that

$$C''(\omega) = \cot(n\pi/2)\, C'(\omega) \propto (i\omega)^{n-1} \qquad (2)$$

i.e. C' and C'' follow the same steeply falling power law in frequency.

Our measurements do not extend to sufficiently low frequencies to enable us to reach definite conclusions about this region, since we cannot see the behaviour of the real part $C'(\omega)$ which should begin to follow a similar upward trend. The loss peak which appears clearly at lower temperatures and higher frequencies gives the impression of being definitely not of the Debye type, since its low-frequency slope is smaller than 1 and its high-frequency part appears almost flat.

The general conclusion is that this Schottky diode gives distinct deviations from the simple behaviour one would associate with a Schottky barrier, i.e. a dc component at low frequencies and a Debye- like loss peak at higher frequencies suggesting an exponentially time-dependent generation-recombination or trapping process in the space charge region.

The temperature dependence of the loss peak and of the quasi-dc component shows distinctly non-Arrhenius behaviour - a plot of the logarithm of the frequency shift against reciprocal temperature $1/T$ is strongly non-linear in both cases, while a linear plot in T is linear over at least part of the available temperature range. This suggests that we are dealing with a significant element

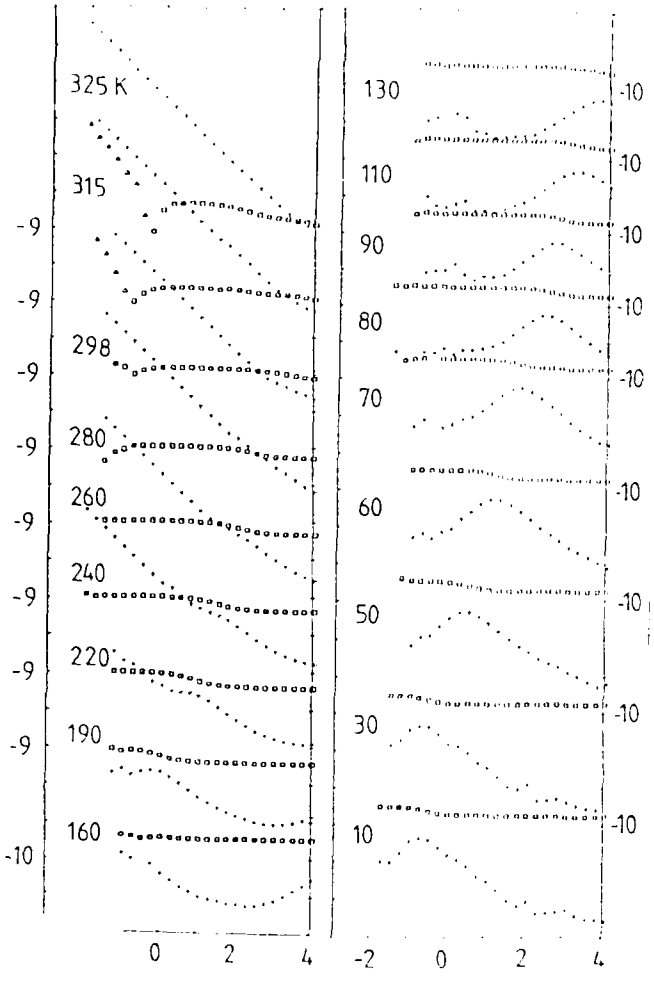

Figure 7

The dielectric response of the silicon surface barrier diode over the temperature range 10 - 325K, showing the progressive evolution of the low- and high-frequency loss processes and of the dc conduction at the higher temperatures. Note the onset of negative capacitance (ΔΔΔΔΔ) at the highest temperatures.

of tunnelling in the electronic transitions involved, which is not surprising. What is more surprising are the deviations from the ideal behaviour in the frequency domain.

A further distinct anomaly may be seen in the variation of the low-frequency loss with temperature at the lower temperatures, where even a superficial examination of the data in Figure 3 shows that the position of the data and the consequent position of the minimum do not follow a regular trend. A distinct minimum of the loss component is seen in this region at approximately 50K, suggesting a transition between two different regimes of dielectric behaviour.

An interesting feature of the behaviour of this silicon diode is the dependence of the dielectric response at 10K on the amplitude of the applied ac signal which was varied betwen 10 and 100 mV, as shown in **Figure 4**. While there is some loss of resolution at 10 mV, there is no doubt that the quasi-dc behaviour at the lowest frequencies is eliminated and only the loss peak at the higher frequencies appears to remain. This result indicates the presence of some non-linearity of the electrical response of the diode at 10K below 0.1V amplitude. Unfortunately, our data for the I - V characteristics in Figure 1b) do not extend below 0.1 V so that it is no possible to check on the presence of such a non-linearity. However, it is clear that at 10K a signal amplitude of 0.1 V

represents a "large" perturbation and it is therefore not surprising to find that the response is non--linear. Further work is needed to elucidate this point in more detail.

One other aspect of the dielectric response of the Schottky diode is shown in **Figure 5** where the measurements are given at 0.1V amplitude and with a range of steady biases in the forward and reverse directions. The low-frequency quasi-dc component increases with forward bias and decreases for —0.14V bias, only to rise again at 0.28 V. This behaviour is as would be expected,

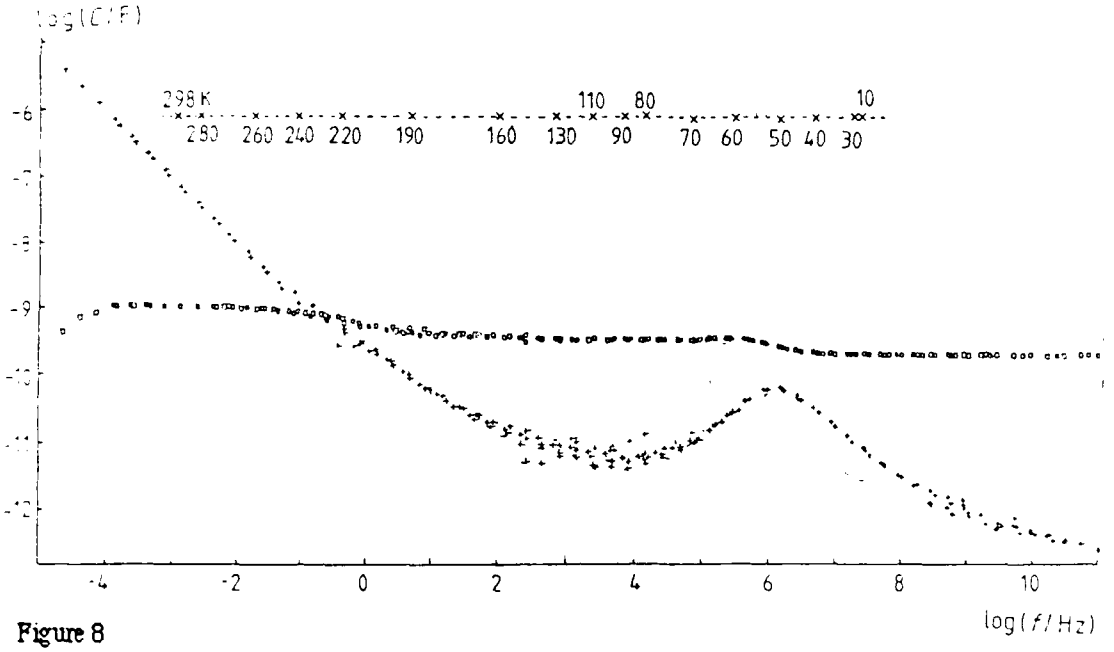

Figure 8

Normalisation of the data of Figure 7 with respect to temperature, with the exception of the three highest temperatures where the behaviour is complicated by the appearance of the negative capacitance, showing the locus of the displacement of the characterisitic point along the frequency axis. The mismatch at the trough between the loss peak and the lower-frequency part is due to the difference in the respective activation energies.

with a rather "soft" reverse characteristic , as seen in Figure 1b). Similar dielectric behaviour was observed at 10, 50 and 70K.

The important point is that none of the causes which change the quasi-dc behaviour appear to have any effect on the higher-frequency loss peak , confirming that these are quite separate processes, as might have been expected. In particular, the spectral shape and position of the loss peak in frequency does not appear to move with the application of a steady bias.

Silicon surface barrier diode

Our next device is a surface barrier diode consisting of a silicon wafer of 1,000 Ωcm n-type material, with a gold Schottky barrier contact and an aluminium back ohmic contact. This is similar in nature to the Schottky diode discussed above except for a much higher resistivity of the base material, the doping density from the plot of $1/C^2$ vs V being $1.5\ 10^{12}\ cm^{-3}$ which is three order of magnitude lower than in the former. The contact barrier is0.45 V. The complete current-voltage characteristic is shown in **Figure 6a)** and the forward branch is shown in semi-logarithmic

representation in diagram b), both at 260K. The latter gives an ideality factor $n = 1.2$, which is not far from the ideal behaviour. The reverse current is significantly lower than in the Schottky diode.

The dielectric response is shown in **Figure 7** over an extended temperature range 10 - 325K, with an amplitude of 0.1V. Starting at the lowest temperatures, we note the presence of a well-defined loss peak with a distinctly broader-than-Debye shape going over at the lowest temperatures and highest frequencies into an almost flat loss. The peak moves to higher frequencies with rising temperature and its low-frequency side develops into a plateau from which a second loss peak emerges between 160 and 220K . Both peaks are clearly associated with the corresponding increments of $\mathcal{C}'(\omega)$, but the lower-frequency peak is rapidly overtaken by what appears to be a dc process - constant $\mathcal{C}'$ and $\mathcal{C}'' \propto \omega^{-1}$. A new trend sets in at 280K with a reduction of the magnitude of the capacitance $\mathcal{C}'(\omega)$ and its eventual change of sign into negative values, plotted as ΔΔΔΔ in the diagram. This trend is well developed at 325 K and it is closely similar to the behaviour reported on GaAs Schottky diodes by Zaidi and Jonscher in the reference quoted.

A complete normalisation of these data, with the exception of the two highest temperatures, is shown in **Figure 8** together with the locus of the displacement point along the frequency axis. It is noteworthy that the normalisation could be carried out with only horizontal translation, meaning that only the time rates of the processes in question were changing with frequency, while no change could be observed in the amplitude. Starting at the high-temperature, low-frequency end, the entire response may be divided into the negative capacitance region which is not shown here, the dc region, the dielectric loss region following on the dc regime and showing an associated clear dispersion of $\mathcal{C}'(\omega)$, the loss peak region and the high-frequency "tail". Because of the different activation energies of the various parts of the spectrum, the normalisation is not always very "neat" , especially in the trough below the loss peak. The peak itself is deviating distinctly from the Debye shape and the high-frequency tail reveals the presence of some processes which are of a very different type. Activation energy plots obtained from the displacement locus, which we are not reproducing here, show an energy of 0.05 eV for the low-temperature high-frequency peak and 0.46 eV for the high-temperature peak which is merging with the dc process with an activation energy of 0.60 eV.

We note the intriguing and unexpected property of the loss process showing a transition from dc transport at the lowest frequencies to a slightly less rapidly changing dependence at just the frequency where the loss intersects the real part $\mathcal{C}'(\omega)$. This type of behaviour was already observed earlier by Zaidi and Jonscher on GaAs Schottky diodes and was attributed by them to some coupling mechanism between the "true" dc process and the distinctly separate low-frequency dielectric process. We are not yet in a position to understand fully this behaviour but it is instructive to note that it can be observed both in the compound and the elemental semiconductors.

An important result of this coupling is the fact that the temperature dependences of the dc and dielectric processes, which are different at lower temperatures, become more nearly equal, so that the respective responses move "in step" with one another beyond a critical temperature.

The effect of forward and reverse bias on the dielectric spectrum of the surface barrier diode at 298K is shown in **Figure 9** , with the clear implication that the negative capacitance region is enhanced and moved to higher frequencies with increasing forward bias, while reverse bias causes its displacement towards lower frequencies and its eventual replacement with strong Low Frequency

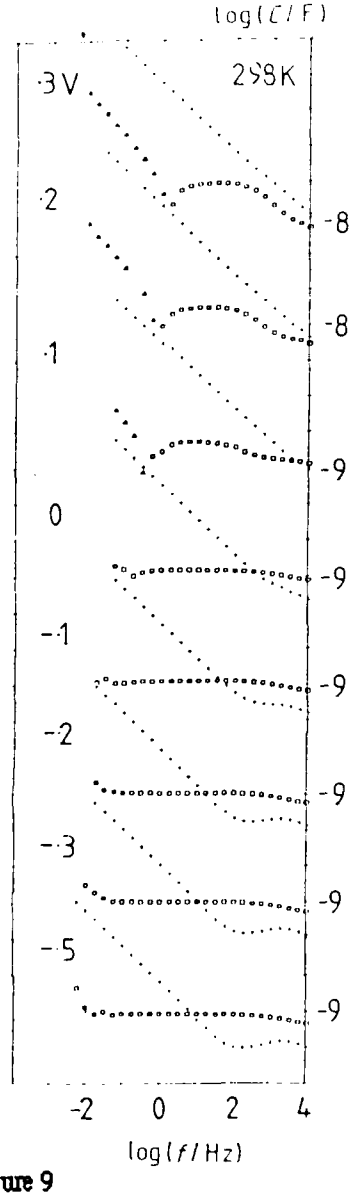

Figure 9

The response of the surface barrier diode at 298K with forward and reverse bias as parameter. Note the transition from negative capacitance to low frequency dispersion.

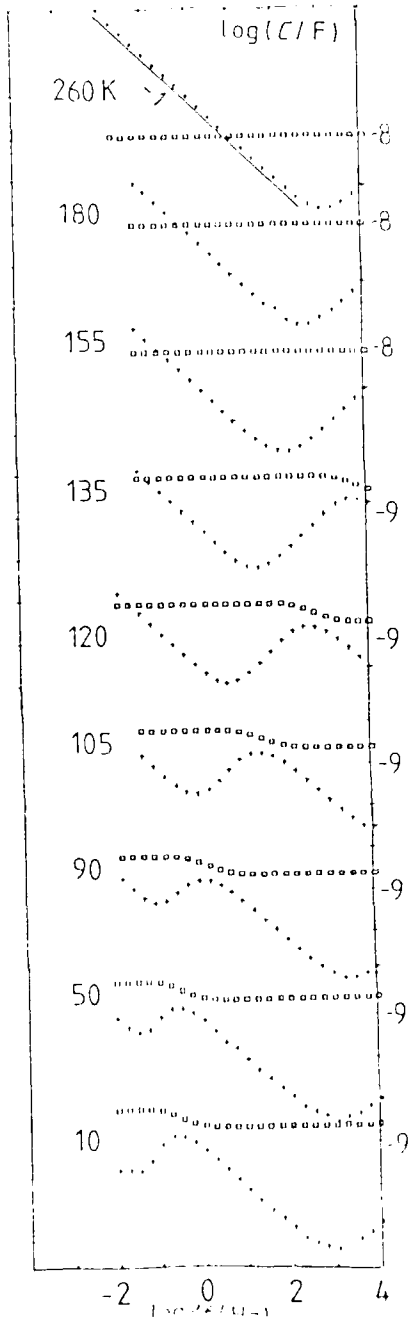

Figure 10

The dielectric response of the silicon n⁺-p junction diode in the temperature range 10-260K

Dispersion (LFD). Very similar behaviour has been described in the context of GaAs Schotky diodes by Zaidi and Jonscher. It is noteworthy that the increment $\Delta C(\omega)$ increases strongly with forward bias, before being overtaken by the negative capacitance trend. This is compatible with the analysis given by Zaidi and Jonscher.

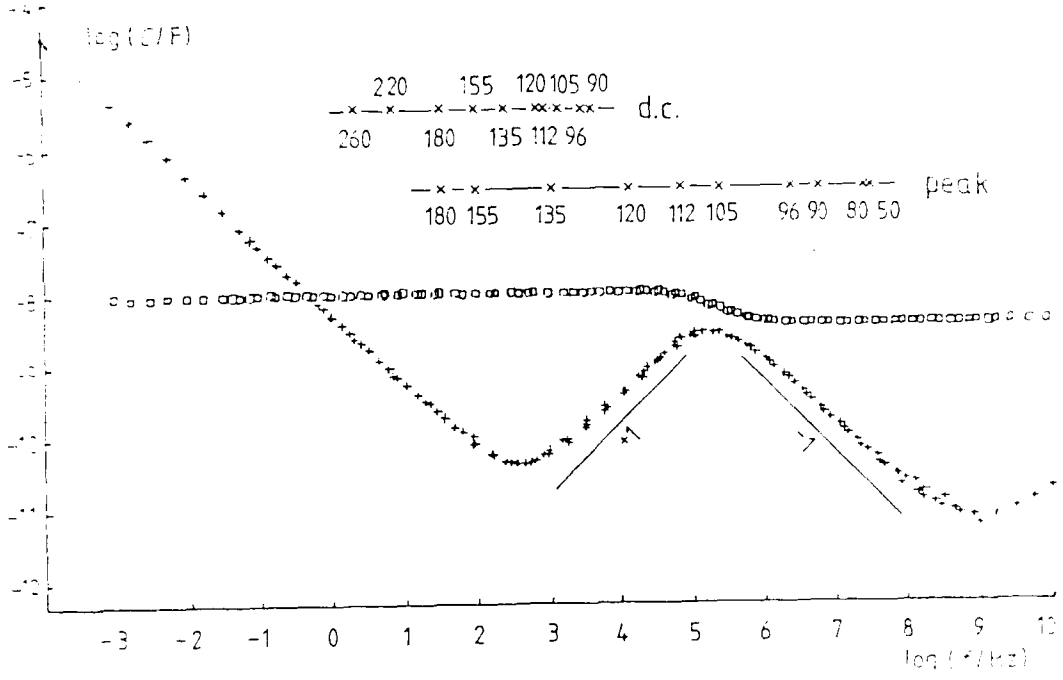

Figure 11

Normalisation of the data of Figure 10 for the silicon p-n junction diode, with two separate fittings for the loss peak and the dc process, at low- and high temperatures, respectively. The corresponding activation energies in the upper reaches of the respective ranges, are 0.12 eV for the dc process and 0.22 eV for the loss peak - a rather unusual behaviour. At lower temperatures there is the usual reduction of the activation slopes, indicating an increasing importance of tunnelling processes.

Silicon n^+ - p junction diode

This device is a large-area nuclear particle detector diode constructed on 3,000 Ωcm p-type silicon with a diffused n^+-type region and a gold back contact. The current-voltage characteristics of this diode show some anomalies at low temperatures, in that the forward branch at 180K is exponential with a non-ideality factor $n = 13$, while at 76K the behaviour appears to be ohmic and to be dominatedby a high resistance of the order of 1 GΩ, which might be compatible with the resistance of the 3,000 Ωcm material at the low temperature in question. The $1/C^2$ vs V curves give a doping density of $4\ 10^{12}$ cm^{-3} which is consistent with the nominal resistivity of the material. The dielectric spectra of this diode are shown in **Figure 10** for the temperature range 10 - 260K and their normalisation is shown in **Figure 11**.

The entire response is made up of only two features - a loss peak and a dc-like behaviour at low frequencies and high temperatures. In contrast with the Schottky responses, there is no trace of any dielectric dispersion below the dc process, which manifests itself by the change of the slope of the loss when crossing the $C''(\omega)$ characteristic. Likewise, there is no trace of negative capacitance or LFD. The rise of loss at the highest frequencies and lowest temperatures may be consistent with the presence of some series resistance in the system.

We note that the I - V characteristic at 76 K showed a series resistance of 1 GΩ which, with the junction capacitance of approximately 1 nF would give a loss peak frequency of 1 Hz, which is in broad agreement with the data in Figure 10. This cannot be the mechanism of the observed loss peak, however, since the capacitance at the higher frequencies should have fallen to a very low value consistent with some stray capacitance of the system, which is manifestly not the case. We must conclude, therefore, that the loss peak is a genuine response of the junction diode and that there is no apparent series resistance.

Discussion of Results

A summary of the principal experimental parameters is given in Table I.

Our experimental results reveal some important points about the contrasting spectroscopic behaviour of Schottky diodes and p-n junctions and they constitute an extension of the previous findings relating to GaAs Schottky diodes. It should be noted that our surface barrier and p-n junction data refer to high-resistivity silicon, 1,000 and 3,000 Ωcm, respectively, while the silicon Schottky diode is on much lower resistivity material, approximately 10 Ωcm.

The most important common features are the appearance in all three cases of a distinct loss peak which is nearly symmetric and deviates only slightly from the Debye shape for the surface barrier diode and the p-n junction diode on high-resistivity materials, while the Schottky diode on the low resistivity material has a much less Debye-like shape. It would appear that the low resistivity of the base material has something to do with increasing deviations from Debye shape. On the other hand, this peak is very similar in Schotkky and p-n junction diodes, confirming that it must be connected with the space charge region rather than with the interface. This is in agreement with the fact that the loss peak is not affected by steady bias and the capacitance increment associated with the loss peak is of a magnitude consistent with the space charge region and not with that of the bulk base material, which would be very much smaller.

A loss peak with its corresponding increment of $C'(\omega)$ is evidence of "dipole-like" processes, i.e. ones in which there is a strictly limited displacement of charge but without a continuing transport process which leads to dc conduction. In the context of the space charge region of a p-n junction or a Schottky diode this implies an electronic transition from a deep level into the conduction band, or between two localised levels, but in either case there is no follow-up by replenishment of the level just vacated. The process of emission into the free band is likely to be thermally activated,a transition between two localised levels is more likely to involve a significant element of tunnelling. We must conclude that the processes seen in the Schottky barrier on low-resistivity silicon are tunnelling between localised levels within the space charge region, while those involved in the high-resistivity materials, both surface barrier and p-n junction, are more likely the emission from localised levels into the conduction - or valence - band. The 0.05 eV energy in the case of the surface barrier diode might be attributed to donor activation energy, except for the fact that in a material of 10^3 Ωcm room temperature resistivity the Fermi level does not approach the donor levels until 20K, or so, hence these levels are empty at the temperatures where the loss peak is most pronounced. We conclude, therefore, that the electronic transition giving rise to the less peak is not emission into the conduction band but it must be associated with neighbouring deeper levels at the position where the Fermi level cuts these, so that some are full and some empty. Since, in the absence of an electric field the levels

are at the same energy, the transitions in question must involve neighbouring levels whose energies are split by the field in the space charge region.

One difficulty with this interpretation is the inevitable distribution of possible spacings which may be expected in a real material with a random distribution of centres and with a distribution of angles between the pairs of centres and the electric field in the space charge region. This would imply that there should be a considerable broadening of the loss peak, compared with the Debye shape and, while we do find a slight broadening, this seems too narrow for such a haphazard process. At the moment we do not have any further explanations of this aspect of our results.

The second difficulty is that the magnitude of polarisation increment $\Delta C'$ which is possible to expect from a nearest-neighbour jump between deep levels is very small - certainly much smaller than the polarisation arising from the emission of an electron from a deep level into the conduction band, which results in a much larger displacement, i.e. a much larger dipole moment.

A fundamental feature of the Schottky barrier on the high-resistivity surface barrier diode is the clear appearance of the secondary strongly dispersive low-frequency loss peak process which merges into the dc conduction process. This is almost certainly intimately connected with the LFD and negative $C'(\omega)$ phenomena which were found by Zaidi and Jonscher to be characteristic of the behaviour of GaAs Schottky diodes and were attributed to interfacial processes. Their total absence in p-n junctions has been commented on previously and it is now very interesting to note that they are seen likewise in silicon Schottky diodes, although they could not be observed in the low-resistivity diode described here on account of it too high dc conductance which made it impossible to measure the dielectric behaviour at temperatures in which these processes become observable.

This means that the interfacial LFD and negative capacitance behaviour is *not* confined to compound semiconductor interfaces and this establishes a better basis for the interpretation and understanding of the mechanisms involved. The fact that these processes are strongly dependent on even relatively slight forward and reverse bias suggests that we are concerned here with transport of ionic species towards and away from the interface, with consequent formation or removal of oxide. This would then condition the electrochemical response of the system in a manner which leads to the appearance of one or other of the types of behaviour.

Conclusions

The experimental results reported here for Schottky diodes and p-n junctions on silicon provide significant new information about the dynamic processes involving electronic transitions between localised states in the space charge regions and at the interfaces of the Schottky barriers. More work is required with carefully characterised devices to obtain a detailed understanding of the processes in question, which could lead to better diagnostic techniques for the assessment of device materials.

We require, in particular, a better understanding of the true nature of the LFD and negative capacitance processes - which we believe to be related in their physical origins. We need to understand any electrochemical implications of these, which appear to be very likely in the light of our past experience. The question of possible "coupling" between the true dc transport and the strongly dispersive loss peak process that follows it in the high-resistivity surface barrier diode is also very intriguing. It is possible, of course, that the dc process arising from some form of

excitations of charge carriers from deep levels in the space charge region of the diode contains an inevitable element of dielectric response which is closely linked with it, but this is only a qualitative description of a process that has to be understood more quantitatively.

A highly important element of the behaviour of all three devices described in this Report is the high-frequency loss peak the mechanism of which cannot at present be said to have been identified. Being a bulk process, albeit limited to the space charge region, This process is bound to have a high diagnostic potential.

Table I

Summary of results

Device	Schottky	Surface barrier	p-n$^+$ junction
base material (Ωcm at room temp.)	p ≈10	n $3\,10^3$	p $1\,10^3$
impurity density	$\approx 10^{16}$	$\approx 10^{12}$	$\approx 3\,10^{11}$
ideality factor (room temperature)	1.0	1.2	
loss peak shape	deviates from Debye	near-Debye	near-Debye
loss peak frequency at 50K (Hz)	10^3	3	0.3
loss peak activation energy (eV)	evidence of tunnelling	0.05	0.224
dc activation energy (eV)	evidence of tunnelling	0.46	0.12
low-frequency high-temperature	no evidence of LFD or -ve C' up to 210K, above too conducting	-ve C' and LFD T > 300K with influence of bias	no -ve C' nor LFD
special features	loss dependent on signal amplitude, decreasing below 10 mV.	secondary low-frequency loss peak coupled to dc process	


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